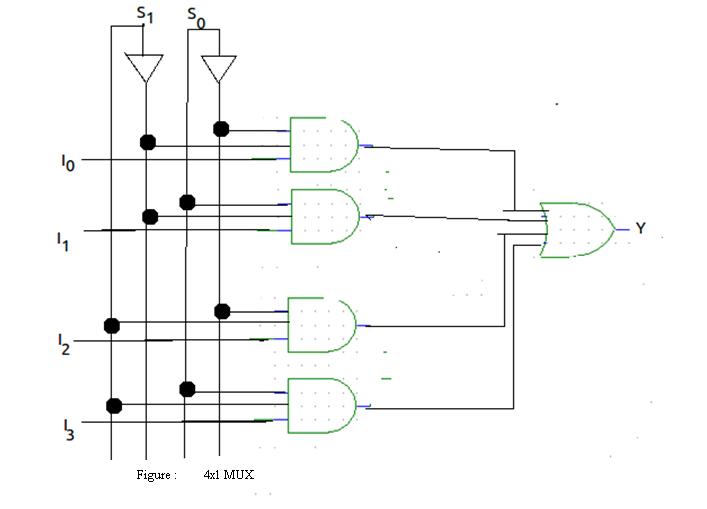
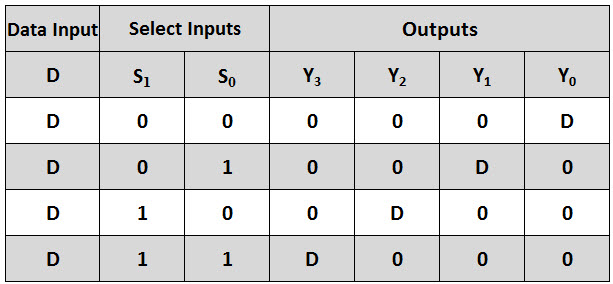
**Circuit Diagram & Truth Table:**



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**Code:**

* **Design Module**

module mux(out,a,b,c,d,s0,s1);

input a,b,c,d,s0,s1;

output out;

reg out;

always @(a or b or c or d or s0 or s1)

begin

case({s0,s1})

2'b00: out=a;

2'b01: out=b;

2'b10: out=c;

2'b11: out=d;

endcase

end

endmodule

* **TestBench**

module Baig;

reg a,b,c,d,s0,s1;

wire out;

mux m(out,a,b,c,d,s0,s1);

initial

begin

a=1'b0;b=1'b1;c=1'b0;d=1'b1;s0=1'b0;s1=1'b0;

#30

s0=1'b0;s1=1'b1;

#30

s0=1'b1;s1=1'b0;

#30

s0=1'b1;s1=1'b1;

#30

$finish;

end

endmodule

**Output:**

Graphical user interface, application, table

Description automatically generated